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Article in *Applied Physics Letters* · April 2011

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Reduced surface leakage current and trapping effects in AlGaIn/GaN high electron mobility transistors on silicon with SiN/Al₂O₃ passivation

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(Received 23 February 2011; accepted 28 February 2011; published online 17 March 2011)

The surface leakage currents and the surface trapping effects of the AlGaIn/GaN high electron mobility transistors (HEMTs) on silicon with different passivation schemes, namely, a 120 nm plasma enhanced chemical vapor deposited SiN, a 10 nm atomic layer deposited (ALD) Al₂O₃ and a bilayer of SiN/Al₂O₃ (120/10 nm) have been investigated. After SiN passivation, the surface leakage current of the GaN HEMT was found to increase by about six orders; while it only increased by three orders after the insertion of Al₂O₃ between SiN and AlGaIn/GaN. The surface conduction mechanism is believed to be the two-dimensional variable range hopping for all the samples. The leakage current in the etched GaN buffer layer with SiN/Al₂O₃ bilayer passivation was also much smaller than that with only SiN passivation. The pulse measurement shows that the bilayer of SiN/Al₂O₃ passivation scheme can effectively reduce the surface states and suppress the trapping effects. © 2011 American Institute of Physics. [doi:10.1063/1.3567927]

The GaN high electron mobility transistor (HEMT) has been demonstrated to be a promising candidate for high power amplifiers in the microwave communication system and high-voltage power switches.^{1,2} Surface passivation is generally necessary to suppress the serious trapping effects such as current collapse and dc-to-rf dispersion due to the large surface states in GaN HEMTs.³ SiN grown by plasma enhanced chemical vapor deposition (PECVD) system is widely used as the surface passivation dielectric and has been demonstrated to be an effective material to reduce the surface states on GaN or AlGaIn.³ However, The surface leakage current of the GaN HEMT after PECVD SiN passivation depends on the deposition conditions, and it has been observed to obviously increase after passivation.^{4,5}

Recently the Al₂O₃ grown by atomic layer deposition (ALD) system has attracted great interests in the application of GaN metal-insulator-semiconductor HEMTs due to its high dielectric constant, high breakdown field, excellent uniformity and good quality.^{6–8} It has also been demonstrated to be used as a surface passivation layer in the GaN HEMT.^{9,10} We have observed that a thin ALD Al₂O₃ layer used for the gate dielectric and passivation can increase the 2-dimensional-electron-gas sheet carrier density and drift mobility through the suppression of the trapping effect.¹¹ In this letter, we report that the high surface leakage current in the GaN HEMT caused by the PECVD SiN passivation can be reduced by inserting a thin ALD Al₂O₃ layer.

The GaN HEMT structure is shown in Fig. 1. It was grown on a high-resistivity silicon substrate (>6000 Ω cm) by metal-organic chemical vapor deposition. Its epilayer includes a 2 nm unintentionally doped GaN cap layer, a 17.5 nm Si-doped AlGaIn barrier layer, a 1.2 nm AlN spacer layer and a 1.5 μm undoped GaN buffer. The fabrication details of the GaN HEMT can be found elsewhere.⁷ The device surface was passivated and the electrodes were opened by etching away the dielectric for measurement. Four

samples with different passivation schemes were studied: Sample A, without passivation; Sample B, passivated with 120 nm PECVD SiN; Sample C, passivated with 10 nm ALD Al₂O₃; Sample D, passivated with a bilayer of 10 nm ALD Al₂O₃ and 120 nm PECVD SiN. Before passivation, the surface of the samples were carefully treated using ultrasonic acetone and isopropyl alcohol followed by buffered oxide etchant (HF:NH₄F=1:6.4). The PECVD SiN was deposited with SiH₄:NH₃=2:3 at rf power of 20 W and at 300 °C; and the ALD Al₂O₃ was deposited with trimethylaluminum and H₂O as precursors at 300 °C. The dc and pulsed current-voltage (*I*-*V*) measurement were carried out using an HP 4156 semiconductor parameter analyzer and a Diva pulse measurement system, respectively.

The surface leakage currents of the GaN HEMTs with various passivation schemes were measured using the double-gate devices. The circuit configuration for the measurement is shown in Fig. 1(a), similar to the technique reported in Ref. 12. The distances from gate 1 to gate 2 and from gate 2 to drain are 3 μm and 2 μm, respectively. The gate length and width are 1 μm and 50 μm, respectively.

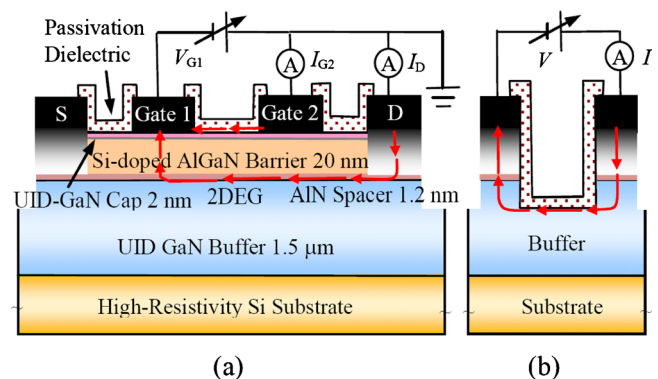


FIG. 1. (Color online) (a) Schematic of the passivated AlGaIn/GaN HEMT with double gate and the circuit configuration for surface leakage current measurement; (b) schematic of the circuit configuration for etched GaN buffer leakage current measurement.

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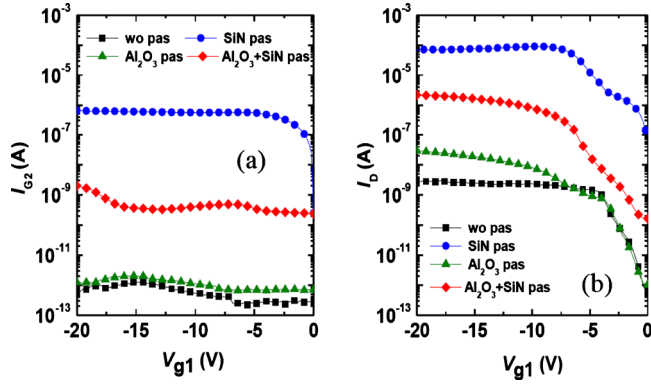


FIG. 2. (Color online) (a) The surface leakage current (I_{G2}) and (b) vertical leakage current (I_D) of the double-gate GaN HEMTs with various passivation schemes under the measurement configuration in Fig. 1.

During the measurement, the gate 2 and drain were biased at 0 V, and the gate 1 was swept from 0 to -20 V. The measurement of the etched GaN buffer leakage current was from two Ohmic contact electrodes fabricated on the AlGaIn/GaN mesa with a gap of 5 μm and width of 50 μm , as shown in Fig. 1(b). Between the two electrodes, the AlGaIn/GaN was etched down to a depth around 200 nm.

Figure 2 shows the measured vertical leakage current (I_D) and surface leakage current (I_{G2}). For comparison, the values of the currents at $V_{g1} = -20$ V for four samples have also been listed in Table I. Compared to the device without passivation, the SiN passivation has increased the surface leakage current up to six orders. However, the device passivated with 10 nm Al_2O_3 has a similar value of surface leakage current compared to the unpassivated device. The surface leakage current of the device passivated with the SiN/ Al_2O_3 bilayer is three orders larger than those of the devices unpassivated and passivated with Al_2O_3 , but three orders smaller than that of the device passivated with only SiN. This means that the surface leakage current of the device with bilayer passivation neither flows along the Al_2O_3 /nitride semiconductors interface, nor along the Al_2O_3 bulk, but along the SiN bulk. The 10 nm Al_2O_3 has blocked part of current injected from the SiN layer to the gate. It can be expected that a thicker Al_2O_3 can further suppress the surface leakage current in the bilayer passivated device.

The vertical leakage current was also observed to increase after passivation, as shown in Fig. 2(b). For all the samples, the magnitude of I_D is at least one order larger than that of I_{G2} , indicating that the gate leakage current of the GaN HEMTs is mainly from the vertical path, namely, the Schottky leakage current, instead of the surface path. The increase in the vertical leakage current after passivation is believed to be due to the enhanced electrical line crowding at the drain side of the gate. Similar to the case of the surface

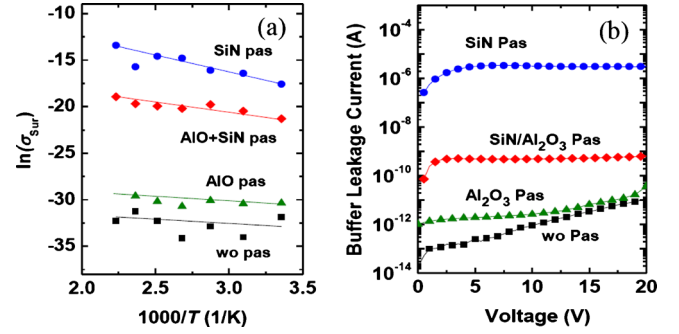


FIG. 3. (Color online) (a) Arrhenius plot of surface leakage conductivity from 25 to 175 $^{\circ}\text{C}$ at $V_{G1} = -20$ V; (b) leakage current of the etched GaN buffer with various passivation schemes.

leakage current, the Al_2O_3 passivated device shows the lowest vertical leakage current among the three passivated devices, whereas the SiN passivated device shows the highest value.

To further investigate the physical origin of the surface leakage current, we carried out the temperature dependent I - V measurement for the double-gate devices from 25 to 175 $^{\circ}\text{C}$. The Arrhenius plot of the surface leakage conductivity σ_{sur} is shown in Fig. 3(a). It can be seen that the devices without passivation and with Al_2O_3 passivation have similar activation energies ($E_a = 0.065$ eV and $E_a = 0.045$ eV, respectively, see Table I). It means that the Al_2O_3 dielectric has not introduced any new surface leakage mechanism. The device with SiN passivation has a much different activation energy $E_a = 0.26$ eV. In CVD prepared amorphous SiN alloy, typically two activation energies E_{a1} , E_{a2} exist in the leakage conductivity, as shown in the following expression:¹³

$$\sigma_{\text{SiN}} = \sigma_1 \exp\left(-\frac{E_{a1}}{k_B T}\right) + \sigma_2 \exp\left(-\frac{E_{a2}}{k_B T}\right),$$

where $E_{a1} > E_{a2}$ and E_{a1} is typically around 0.7–0.8 eV from the extended state conduction. E_{a2} is typically around 0.1–0.2 eV from the hopping conduction through the gap-states near the Fermi level.¹³ The E_a value of 0.26 eV obtained from our measurement shows that, the surface leakage current after PECVD SiN passivation is due to the hopping conduction through the gap-states near the Fermi level in SiN. The device with bilayer passivation has an E_a of 0.14 eV, which is believed to be resulting from the combination of the hopping conduction in SiN and the tunneling conduction across the Al_2O_3 .

We have also found that a straight line can be fit well for the plot of $\ln(\sigma_{\text{sur}})$ versus $T^{1/3}$ for all the four samples (the figures are not shown here). This verifies that the conductiv-

TABLE I. Various characteristics for the GaN HEMTs with different passivation schemes. [I_D , I_{G2} are the values at $V_{g1} = -20$ V; I_{buf} is the value at $V = -20$ V].

Sample No.	Passivation scheme	I_D (mA/mm)	I_{G2} (mA/mm)	E_a (eV)	I_{buf} (mA/mm)	R_{sh} (Ω/sq)	I_{dmax} drop at pulsed dc (%)	R_{on} increase at pulsed dc (%)
A	Without passivation	6.1×10^{-5}	1.0×10^{-8}	0.065	2.1×10^{-7}	367	59	72
B	120 nm PECVD SiN	1.4	1.2×10^{-2}	0.26	6.3×10^{-2}	324	0	0
C	10 nm ALD Al_2O_3	5.9×10^{-4}	2.4×10^{-8}	0.045	6.1×10^{-7}	325	0	14
D	SiN/ Al_2O_3 (120/10 nm)	4.3×10^{-2}	3.9×10^{-5}	0.14	1.4×10^{-5}	328	0	0

ity of the surface leakage follows the two-dimensional variable range hopping model, as the following expression shows:¹²

$$\sigma(T) \propto \exp[-(T_0/T)^{1/3}],$$

where T_0 is the characteristic temperature.

The leakage current of the etched GaN buffer is also important for the actual GaN circuits. Figure 3(b) shows the measured buffer leakage current of the four samples with different passivation schemes. The unpassivated GaN buffer and Al_2O_3 passivated GaN buffer show similar leakage currents at voltage >10 V. The SiN passivation increases the leakage current by more than five orders, and the insertion of a 10 nm Al_2O_3 has lowered down the value by two orders.

To investigate the passivation effect of the various schemes, the sheet carrier resistance (R_{sh}) of the four samples has been measured using van der Pauw patterns, and their values are listed in Table I. The three passivated samples have similar R_{sh} values, which are $\sim 11\%$ smaller than that of the unpassivated samples. In addition, pulsed I - V measurement was performed with pulse width of 200 ns and duty cycle of 0.02%. The I - V characteristics under gate stress bias (e.g., quiescent gate bias $V_{\text{gq}} < V_{\text{th}}$, quiescent drain bias $V_{\text{dq}} = 0$) can be used to check the effect of the surface passivation on the reduction in the surface states.¹⁴ The values of the maximum drain current (I_{dmax}) and on-resistance (R_{on}) at $V_{\text{gq}} = -6$ V, $V_{\text{dq}} = 0$ V have been compared with those values at $V_{\text{gq}} = 0$, $V_{\text{dq}} = 0$ V for all the samples, respectively. The results at $V_{\text{g}} = 0$ V are listed in Table I. It can be seen that, the I_{max} at gate stress has dropped by 59% and R_{on} increased by 72% for the unpassivated device. This indicates the existence of the large-density surface states. The Al_2O_3 passivated device shows no drop of I_{dmax} but 14% increase in R_{on} . Whereas the SiN passivated device and the $\text{Al}_2\text{O}_3/\text{SiN}$ bilayer passivated device show no change in I_{dmax} and R_{on} , indicating that only a thin Al_2O_3 film is not sufficient to serve as a passivation layer. Considering it is time-consuming for the ALD to deposit a thicker Al_2O_3 layer and its higher dielectric constant than SiN, the insertion of a thin ALD Al_2O_3 between the SiN and nitride semiconductor is

proposed to be an appropriate passivation scheme to effectively reduce the surface states without the introduction of large surface leakage current.

In conclusion, the PEDCVD SiN passivation has been found to largely increase the surface leakage current for the GaN HEMT, due to the hopping conduction through the gap-states near the Fermi level with $E_a = 0.26$ eV. The insertion of a thin ALD Al_2O_3 layer between the PECVD SiN and the nitride semiconductors can effectively reduce the surface leakage current, and meantime maintain the effective passivation effect to reduce the surface states.

The authors would like to thank the Defense Science and Technology Agency of Singapore for the support of this work.

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